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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/032,144	ROUSSEL, PATRICE	
	Examiner	Art Unit	
	Tonia LM Dollinger	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 December 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *19-23 and 93-118* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *19-23 and 93-118* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections

1. Two sets of rejections follow.

Claim Rejections - 35 USC § 102-First Set of Rejections

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 19-23, 93-106 and 109-118 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Abdallah et al., US Patent 6,115,8 12 (herein after Abdallah). Referring to claim 19, Abdallah have taught a method comprising:

a. storing a plurality of non-continuous groups of source bits into a plurality of noncontiguous groups of destination storage locations (Figure 3E, column 6, lines 42-55);

b. b. duplicating bits from the plurality of non-contiguous groups of destination bits into groups of destination storage locations contiguous to the non-continuous groups of destination storage locations (Figure 3E, column 6, lines 42-55, When element 354 is BBDD.).

4. Referring to claim 20, Abdallah have taught the method of claim 19, as described above, and in which the source bits are stored in a first register (Figure 3E, column 6, lines 42-55, element 350).

5. Referring to claim 2 1, Abdallah have taught the method of claim 19, as described above, and in which the source bits represent a double-precision floating point value (column 5, lines 26-40, column 4, lines 25-57).

6. Referring to claim 22, Abdallah have taught the method of claim 19, as described above, and in which the source bits are stored in a first memory location (Figure 3E, column 6, lines 42-55, element 350).

7. Referring to claim 23, Abdallah have taught the method of claim 19, as described above, and in which the source bits represent a single-precision floating point value (column 5, lines 26-40, column 4, lines 25-57).

8. Referring to claim 93, Abdallah have taught an apparatus comprising:

a. a first storage area to store a plurality of non-contiguous groups of source bits (Figure 3E, column 6, lines 42-55, elements 350 and 354, When element 354 is BBDD.);

b. a second storage area to store contiguous duplicates of the plurality of noncontiguous groups of source bits (Figure 3E, column 6, lines 42-55, elements 350 and 354, When element 354 is BBDD.).

9. Referring to claim 94, Abdallah have taught the apparatus of claim 93, as described above, and wherein the plurality of non-contiguous groups of source bits are to represent a plurality of 32-bit double-precision floating point value (column 5, lines 26-40, column 4, lines 25-57).

10. Referring to claim 95, Abdallah have taught the apparatus of claim 94, as described above, and wherein the first storage area comprises a 128-bit memory

location (column 5, lines 26-40, column 4, lines 25-57, Figure 3E, element 350, Four times thirty-two equals 128.).

11. Referring to claim 96, Abdallah have taught the apparatus of claim 94, as described above, and wherein the first storage and second storage areas each comprise a 128-bit register (column 5, lines 26-40, column 4, lines 25-57, Figure 3E, elements 350 and 354).

12. Referring to claim 97, Abdallah have taught the apparatus of claim 93, as described above, and wherein the plurality of non-contiguous groups of source bits comprise four single precision floating point values (column 5, lines 26-40, column 4, lines 25-57, Figure 3E).

13. Referring to claim 98, Abdallah have taught the apparatus of claim 93, as described above, and wherein the second storage area is to store only two of the plurality of noncontiguous groups of source bits and their duplicates (Figure 3E, column 6, lines 42-55, elements 3 50 and 3 54, When element 3 54 is BBDD only two are stored.).

14. Referring to claim 99, Abdallah have taught the apparatus of claim 93, as described above, and wherein the first and second storage areas are to store data corresponding to multimedia instructions (column 1, lines 5-55).

15. Referring to claim 100, Abdallah have taught the apparatus of claim 99, as described above, and further comprising an execution unit to execute the multi-media instructions (Figure 1, element 1 12).

16. Referring to claim 101, Abdallah have taught a system comprising:

a. a memory to store a plurality of instructions (Figure 1, element 120);

b. a processor to fetch a first instruction fiom the memory (Figure 1, element 1 lo), wherein the first instruction, if executed by the processor, is to cause the processor to store contiguous duplicates of a plurality of non-contiguous groups of source bits into a plurality of destination storage locations (Figure 3E, column *6,* lines 42-55, When element 354 is BBDD.).

17. Referring to claim 102, Abdallah have taught the system of claim 101, as described above, and wherein the plurality of non-contiguous groups of source bits include a least significant 32 source bits (Figure 3E, column 5, lines 26-40, column 6, lines 42-55, element 350, D).

18. Referring to claim 103, Abdallah have taught the system of claim 10 1, as described above, and wherein the plurality of non-contiguous groups of source bits include a most significant 32 source bits (Figure 3E, column 5, lines 26-40, column 6, lines 42-55, element 350, A).

19. Referring to claim 104, Abdallah have taught the system of claim 102, as described above, and wherein the plurality of non-contiguous groups of source bits include a second most significant group of 32 source bits (Figure 3E, column 5, lines 26-40, column 6, lines 42-55, element 350, A).

20. Referring to claim 105, Abdallah have taught the system of claim 103, as described above, and wherein the plurality of non-contiguous groups of source bits include a second least significant group of 32 source bits (Figure 3E, column 5, lines 26-40, column 6, lines 42-55, element 350, D).

21. Referring to claim 106, Abdallah have taught the system of claim 101, as described above, and wherein the first instruction does not include a code to designate an order in which the plurality of non-contiguous groups of source bits are to be stored into the plurality of destination storage locations (Figure 3E, column 6, lines 42-55).

22. Referring to claim 109, Abdallah have taught the system of claim 101, as described above, and wherein the processor is to fetch a second instruction from the memory (Figure 1, element 110), the second instruction to store a first number of non-contiguous duplicates (Figure 3E, column 6, lines 42-55, When element 354 is DDDD, there are three non-contiguous duplicates i.e. the first and third, the second and fourth and the first and fourth locations.) of a second number of contiguous groups of source bits (Figure 3E, column 6, lines 42-55, When element 354 is DDDD, element 350 only has one contiguous group of source bits.) into a destination storage location (Figure 3E, column 6, lines 42-55, element 354), the first number being larger than the second number (Three is larger than one.).

23. Referring to claim 110, Abdallah have taught a machine-readable medium having stored thereon an instruction, which if executed by a machine, causes the machine to perform a method comprising:

a. storing bits (31-0) of a source value into bit storage locations (63-32) and (31-0) of a destination register (Figure 3E, column 5, lines 26-40, column 6, lines 42-55, element 354 is BBDD),

b. storing bits (95-64) of the source value into bit storage locations (127-96) and (95-64) of the destination register, wherein the instruction does not

include a code to designate the order in which the source bits are to be stored in the destination register (Figure 3E, column 5, lines 26-40, column 6, lines 42-55, element 354 is BBDD).

24. Referring to claim 111, Abdallah have taught the machine-readable medium of claim 110, as described above, and wherein the source value is stored in a memory location (Figure 3E, column 6, lines 42-55, element 350).

25. Referring to claim 112, Abdallah have taught the machine-readable medium of claim 110, as described above, and wherein the source value is stored in a register (Figure 3E, column 6, lines 42-55, element 350).

26. Referring to claim 113, Abdallah have taught a machine-readable medium having stored thereon an instruction, which if executed by a machine causes the machine to perform a method comprising:

a. storing bits (63-32) of a source value into bit storage locations (31-0) and (63-32) of a destination register (Figure 3E, column 5, lines 26-40, column 6, lines 42-55, element 354 is AACC),

b. storing bits (127-96) of the source value into bit storage locations (127-96) and (95-64) of the destination register, wherein the instruction does not include a code to designate the order in which the source bits are to be stored in the destination register (Figure 3E, column 5, lines 26-40, column 6, lines 42-55, element 354 is AACC).

27. Referring to claim 114, Abdallah have taught the machine-readable medium of claim 113, as described above, and wherein the source value is stored in a memory location (Figure 3E, column 6, lines 42-55, element 350).

28. Referring to claim 115, Abdallah have taught the machine-readable medium of claim 113, as described above, and wherein the source value is stored in a register (Figure 3E, column 6, lines 42-55, element 350).

29. Referring to claim 116, Abdallah have taught a machine-readable medium having stored thereon an instruction, which if executed by a machine causes the machine to perform a method comprising:

a. storing only bits (63-32) of a source value into bit storage locations (127-96) and (63-32) of a destination register (Figure 3E, column 5, lines 26-40, column 6, lines 42-55, element 354 is CDCD),

b. storing only bits (31-0) of the source value into bit storage locations (31-0) and (95-64) of the destination register, wherein the instruction does not include a code to designate the order in which the source bits are to be stored in the destination register (Figure 3E, column 5, lines 26-40, column 6, lines 42-55, element 354 is CDCD).

30. Referring to claim 117, Abdallah have taught the machine-readable medium of claim 116, as described above, and wherein the source value is stored in a memory location (Figure 3E, column 6, lines 42-55, element 350).

31. Referring to claim 118, Abdallah have taught the machine-readable medium of claim 116, as described above, and wherein the source value is stored in a register (Figure 3E, column 6, lines 42-55, element 350).

Claim Rejections - 35 USC § 103-First Set of Rejections

32. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

33. Claims 107 and 108 are rejected under 35 U.S.C. 103(a) as being unpatentable over Abdallah et al., US Patent 6,115,812 (herein after Abdallah).

34. Referring to claims 107 and 108, Abdallah has taught the systems of claims 104 and 105, as described above. Abdallah has not taught wherein the first instruction is a MOVSHDUP or a MOVSLDUP instruction. However the difference is only found in the nonfunctional descriptive material and is not functionally involved in the steps recited. The storing would be performed the same regardless of the name of the instruction. Thus this descriptive material will not distinguish the claimed invention from the prior art in terms of patentability, see In re Gulack, 703 F.2d 1381,1385,217 USPQ 401,404 (Fed. Cir. 1983)l In re Lowry, 32 F.3d 1579,32 USPQ2d 1031 (Fed. Cir. 1994). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the instructions be labeled anything, including, MOVSHDUP and MOVSLDUP, because merely labeling the instructions differently from that in the prior art would have been obvious. See Gulack cited above.

Claim Rejections - 35 USC § 102-Second Set of Rejections

35. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -
(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

36. Claims 19,20,22, 93, 98,99, 100, 101, 106 and 109 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Sidwell et al., European Patent Application EP 0 743 594 Al, cited on the information disclosure statement filed on June 9,2003 (herein referred to as Sidwell).

37. Referring to claim 19, Sidwell has taught a method comprising:

a. storing a plurality of non-continuous groups of source bits into a plurality of noncontiguous groups of destination storage locations (Figure 17, see zip2n4v2p, For the purpose of this rejection, the source is four locations, increasing from right to left, V3/V2/V1/V0. The zip2n4v2p instruction is performed on the source to produce a destination with eight locations, increasing from right to left, V3/V3/V1/V1, V2/V2/V0/V0. The bits in source groups V0 and V3, which are non-contiguous since they are located at positions one and four, are loaded into the first location and the seventh location of the destination storage location.); and

b. duplicating bits from the plurality of non-contiguous groups of destination bits into groups of destination storage locations contiguous to the non-continuous groups of destination storage locations (Figure 17, see zip2n4v2p, The V0 bits in the first destination memory location are duplicated into

the second destination storage location. The V3 bits in the seventh destination memory location are duplicated into the eighth destination memory location. Bits located in the first and seventh positions (from the plurality of non-contiguous groups of destination bits) are duplicated into groups of destination storage locations contiguous to the first and seventh positions, i.e. the second and eighth positions.).

38. Referring to claim 20, Sidwell has taught the method of claim 19, as described above, and in which the source bits are stored in a first register (Figure *6,* element 104).

39. Referring to claim 22, Sidwell has taught the method of claim 19, as described above, and in which the source bits are stored in a first memory location (Figure 17, V3/V2/Vl/V0, Figure 1, element 4).

40. Referring to claim 93, Sidwell has taught an apparatus comprising:

a. a first storage area to store a plurality of non-contiguous groups of source bits (Figure 17, see zip2n4v2p, For the purpose of this rejection, the source is four locations, increasing from right to left, V3/V2/Vl/V0. The zip2n4v2p instruction is performed on the source to produce a destination with eight locations, increasing from right to left, V3/V3/V1/V1, V2/V2/V0/V0. The bits in source groups V0 and V3, which are noncontiguous since they are located at positions one and four, are loaded into the first location and the seventh location of the destination storage location.);

b. a second storage area to store contiguous duplicates of the plurality of noncontiguous groups of source bits (Figure 17, see zip2n4v2p, The V0 bits in

the first destination memory location are duplicated into the second destination storage location. The V3 bits in the seventh destination memory location are duplicated into the eighth destination memory location. Bits located in the first and seventh positions (from the plurality of non-contiguous groups of destination bits) are duplicated into groups of destination storage locations contiguous to the first and seventh positions, i.e. the second and eighth positions.).

41. Referring to claim 98, Sidwell has taught the apparatus of claim 93, as described above, and wherein the second storage area is to store only two of the plurality of non-contiguous groups of source bits and their duplicates (Figure 17, Only two duplicates of each source value is stored.).

42. Referring to claim 99, Sidwell has taught the apparatus of claim 93, as described above, and wherein the first and second storage areas are to store data corresponding to multi-media instructions (Figure 17, zip2n4v2p).

43. Referring to claim 100, Sidwell has taught the apparatus of claim 99, as described above, and further comprising an execution unit to execute the multi-media instructions (Figure 1).

44. Referring to claim 101, Sidwell has taught a system comprising:

a. a memory to store a plurality of instructions (Figure 1, page 2, lines 1-38, element 22);

b. a processor to fetch a first instruction from the memory (Figure 1, page 2, lines 1-38, element 8), wherein the first instruction, if executed by the processor, is to cause the processor to store contiguous duplicates of a plurality

of non-contiguous groups of source bits into a plurality of destination storage locations (Figure 17, see zip2n4v2p, For the purpose of this rejection, the source is four locations, increasing from right to left, V3/V2/Vl/V0. The zip2n4v2p instruction is performed on the source to produce a destination with eight locations, increasing from right to left, V3/V3/V1/V1, V2/V2/V0/V0. The bits in source groups V0 and V3, which are non-contiguous since they are located at positions one and four, are loaded into the first location and the seventh location of the destination storage location. The V0 bits in the first destination memory location are duplicated into the second destination storage location. The V3 bits in the seventh destination memory location are duplicated into the eighth destination memory location. Bits located in the first and seventh positions (from the plurality of noncontiguous groups of destination bits) are duplicated into groups of destination storage locations contiguous to the first and seventh positions, i.e. the second and eighth positions.).

45. Referring to claim 106, Sidwell has taught the system of claim 101, as described above, and wherein the first instruction does not include a code to designate an order in which the plurality of non-contiguous groups of source bits are to be stored into the plurality of destination storage locations (Figure 17).

46. Referring to claim 109, Sidwell has taught the system of claim 101, as described above, and wherein the processor is to fetch a second instruction from the memory (Figure 17, zip2n2v4p), the second instruction to store a first number of non-contiguous duplicates (For the purpose of this rejection, the duplicated destination is stored in eight

locations, increasing from right to left, V3/V3/V3/V3, V1/V1/V1/V1. The third position is a non-contiguous duplicate of the first position, the fourth position is a non-contiguous duplicate of the first position, the seventh position is a non-contiguous duplicate of the fifth position and the eighth position is a non-contiguous duplicate of the fifth position. There are at least four non-contiguous duplicates.) of a second number of contiguous groups of source bits (There are only two continuous groups of source bits, V1 and V3.) into a destination storage location (For the purpose of this rejection, the duplicated destination is stored in eight locations, increasing from right to left, V3/V3/V3/V3, V1/V1/V1/V1.), the first number being larger than the second number (Four is larger than two.).

Claim Rejections - 35 USC § 103-Second Set of Rejections

47. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

48. Claims 21, 23, 94,95,96, 97, 102, 103, 104, 105, 107 and 108 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sidwell et al., European Patent Application EP 0 743 594 Al, cited on the information disclosure statement filed on June 9,2003 (herein after Sidwell).

49. Referring to claim 21, Sidwell has taught the instruction of claim 19, as described above. Sidwell has not taught the source bits representing a double floating point data type. However the difference is only found in the nonfunctional descriptive material and

is not functionally involved in the steps recited. The storing would be performed the same regardless of the type of data. Thus this descriptive material will not distinguish the claimed invention from the prior art in terms of patentability, see In re Gulack, 703 F.2d 138 1, 1385,217 USPQ 401,404 (Fed. Cir. 1983). In re Lowry, 32 F.3d 1579, 32 USPQ2d 103 1 (Fed. Cir. 1994). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the source bits represent any type of data, including double floating point, because merely labeling the type differently from that in the prior art would have been obvious. See Gulack cited above.

50. Referring to claim 23, Sidwell has taught the instruction of claim 19, as described above. Sidwell has not taught the source representing a single-precision floating point data type. However the difference is only found in the nonfunctional descriptive material and is not functionally involved in the steps recited. The storing would be performed the same regardless of the type of data. Thus this descriptive material will not distinguish the claimed invention from the prior art in terms of patentability, see In re Gulack, 703 F.2d 1381, 1385, 217 USPQ 401, 404 (Fed. Cir. 1983) In re Lowry, 32 F.3d 1579, 32 USPQ2d 1031 (Fed. Cir. 1994). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the source represent any type of data, including single-precision floating point, because merely labeling the type differently from that in the prior art would have been obvious. See Gulack cited above.

51. Referring to claim 94, Sidwell has taught the apparatus of claim 93, as described above. Sidwell has not taught the source bits representing a double-precision floating point data type. However the difference is only found in the nonfunctional descriptive material and is not functionally involved in the steps recited. The storing would be performed the same regardless of the type of data. Thus this descriptive material will not distinguish the claimed invention from the prior art in terms of patentability, see In re Gulack, 703 F.2d 1381, 1385,2 17 USPQ 401,404 (Fed. Cir. 1983)l In re Lowry, 32 F.3d 1579,32 USPQ2d 103 1 (Fed. Cir. 1994). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the source bits represent any type of data, including double-precision floating point, because merely labeling the type differently from that in the prior art would have been obvious. See Gulack cited above.

52. Furthermore, Sidwell has not taught that the plurality of non-contiguous groups of source bits is to represent a 32 bit value. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the plurality of non-contiguous groups of source bits of Sidwell be any number of bits, including 32-bits, since it has been held that a change in size is not a patentable difference. See In re Rose, 220 F.2d 459,463, 105 USPQ 237,240 (CCPA 1955).

53. Referring to claim 95, Sidwell has taught the apparatus of claim 94, as described above. Sidwell has not taught wherein the first storage area comprises a 128-bit memory location. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the first storage area of Sidwell be any number of

bits, including 32-bits, since it has been held that a change in size is not a patentable difference. See In re Rose, 220 F.2d 459, 463, 105 USPQ 237,240 (CCPA 1955).

54. Referring to claim 96, Sidwell has taught the apparatus of claim 94, as described above. Sidwell has not taught wherein the first storage and second storage areas comprises a 128-bit memory location. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the first storage and second storage areas of Sidwell be any number of bits, including 128-bits, since it has been held that a change in size is not a patentable difference. See In re Rose, 220 F.2d 459,463, 105 USPQ 237,240 (CCPA 1955).

55. Referring to claim 97, Sidwell has taught the apparatus of claim 93, as described above. Sidwell has not taught wherein the plurality of non-contiguous groups of source bits comprise four single-precision floating point values. However the difference is only found in the nonfunctional descriptive material and is not functionally involved in the steps recited. The storing would be performed the same regardless of the type of data. Thus this descriptive material will not distinguish the claimed invention fRom the prior art in terms of patentability, see In re Gulack, 703 F.2d 1381, 1385,217 USPQ 401,404 (Fed. Cir. 1983) In re Lowry, 32 F.3d 1579,32 USPQ2d 103 1 (Fed. Cir. 1994). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the source represent any type of data, including single-precision floating point, because merely labeling the type differently from that in the prior art would have been obvious. See Gulack cited above. Furthermore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the

plurality of non-contiguous groups of source bits of Sidwell comprise any number of values, including four, since it has been held that a change in size is not a patentable difference. See In re Rose, 220 F.2d 459,463,105 USPQ 237,240 (CCPA 1955). Referring to claims 102, 103, 104 and 105, Sidwell has taught the system of claim 101, as described above. Sidwell has not taught wherein the plurality of non-contiguous groups of source bits include: a least significant 32 source bits, a most significant 32 source bits, a second most significant group of 32 source bits and a second least-significant group of 32 source bits. However the difference is only found in the nonfunctional descriptive material and is not functionally involved in the steps recited. The storing of data would be performed the same regardless of the data. Thus this descriptive material will not distinguish the claimed invention from the prior art in terms of patentability, see In re Gulack, 703 F.2d 138 1, 1385, 217 USPQ 401,404 (Fed. Cir. 1983) In re Lowry, 32 F.3d 1579, 32 USPQ2d 103 1 (Fed. Cir. 1994).

56. Referring to claims 107 and 108, Sidwell has taught the systems of claims 104 and 105, as described above. Sidwell has not taught wherein the first instruction is a MOVSHDUP or a MOVSLDUP instruction. However the difference is only found in the nonfunctional descriptive material and is not functionally involved in the steps recited. The storing would be performed the same regardless of the name of the instruction. Thus this descriptive material will not distinguish the claimed invention from the prior art in terms of patentability, see In re Gulack, 703 F.2d 1381,1385,217 USPQ 401,404 (Fed. Cir. 1983) In re Lowry, 32 F.3d 1579, 32 USPQ2d 103 1 (Fed. Cir. 1994).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the instructions be labeled anything, including, MOVSHDUP and MOVSLDUP, because merely labeling the instructions differently from that in the prior art would have been obvious. See Gulack cited above.

Response to Arguments

57. Applicant's arguments filed 12/10/2007 have been fully considered but they are not persuasive.

58. On page 8, Applicant argues in essence:

> *"Abdallah does not recite moving data from a source into non-contiguous destination locations and duplicating them into contiguous destination storage locations, as claimed by Applicant. Instead Abdallah merely moves source data into the destination register into contiguous locations and does not then duplicate the data moved into the contiguous locations, as claimed by applicant. Therefore, Abdallah does not teach that which applicant has claimed."*

However, as in claim 19, Abdallah has taught:

a. storing a plurality of non-continuous groups of source bits into a plurality of noncontiguous groups of destination storage locations (Figure 3E, column 6, lines 42-55, where B and D are non-contiguous in the source bits. These non-contiguous source bits are stored in non-contiguous locations (first and third locations) of the destination.);

b. duplicating bits from the plurality of non-contiguous groups of destination bits into groups of destination storage locations contiguous to the non-continuous groups of destination storage locations (Figure 3E, column 6, lines 42-55, When element 354 is BBDD. The values in the first and third bit locations are duplicated into the second and fourth bit locations. The first

location is contiguous to the second and the third location is contiguous to the fourth location.).

Therefore Abdallah has in fact taught that which Applicant has claimed. Therefore this argument is moot.

59. On page 8, Applicant argues in essence:

"Sidwell does not teach or suggest the limitation of moving data from a source into non-contiguous destination locations and duplicating them into contiguous destination storage locations, recited in these independent claims. No other reference was cited to cure those deficiencies of Sidwell."

However, as in claim 19, Sidwell has taught:

a. storing a plurality of non-continuous groups of source bits into a plurality of noncontiguous groups of destination storage locations (Figure 17, see zip2n4v2p, For the purpose of this rejection, the source is four locations, increasing from right to left, V3/V2/V1/V0. The zip2n4v2p instruction is performed on the source to produce a destination with eight locations, increasing from right to left, V3/V3/V1/V1, V2/V2/V0/V0. The bits in source groups V0 and V3, which are non-contiguous since they are located at positions one and four, are loaded into the first location and the seventh location of the destination storage location.); and

b. duplicating bits from the plurality of non-contiguous groups of destination bits into groups of destination storage locations contiguous to the non-continuous groups of destination storage locations (Figure 17, see zip2n4v2p, The V0 bits in the first destination memory location are duplicated into the second destination storage location. The V3 bits in the seventh destination

memory location are duplicated into the eighth destination memory location. Bits located in the first and seventh positions (from the plurality of non-contiguous groups of destination bits) are duplicated into groups of destination storage locations contiguous to the first and seventh positions, i.e. the second and eighth positions.).

So Sidwell has in fact taught moving data from a source into non-contiguous destination locations and duplicating them into contiguous destination storage locations, as recited in these independent claims. Therefore this argument is moot.

Conclusion

60. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

61. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

62. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tonia LM Dollinger whose telephone number is (571)

272-4170. The examiner can normally be reached on Monday-Friday with first Friday's off.

63. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alford Kindred can be reached on (571) 272-4037. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

64. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

TLMD

/Tonia LM Dollinger/
Primary Examiner, Art Unit 2181
February 28, 2008